One Micron Damascene Redistribution for Fan-Out Wafer Level Packaging using a Photosensitive Dielectric Material

Warren W. Flack, Robert Hsieh, Ha-Ai Nguyen
Ultratech, a division of Veeco
3050 Zanker Road, San Jose, CA 95134 USA
wflack@ultratech.com

John Slabbekoorn, Samuel Suhard, Andy Miller
IMEC
Kapeldreef 75 B-3001 Leuven, Belgium
John.Slabbekoorn@imec.be

Akito Hiro, Romain Ridremont
JSR MICRO NV
Technologielaan 8 B-3001 Leuven, Belgium
akito.hiro@jsrmicro.be

Abstract

This study investigates creation of 1.0µm RDL structures by a damascene process utilizing a photosensitive permanent dielectric material. The advantage of the photosensitive dielectric approach is that the Cu overburden removal does not affect the quality of the embedded Cu lines. In comparison, for a semi-additive process the Cu seed etch affects the final dimensions of the RDL lines [1]. Damascene processing of RDL will also result in a flat wafer surface which greatly improves the lithographic performance for subsequent layers. Finally, the Cu line is surrounded on the sides and bottom by a Ti barrier layer which provides a Cu diffusion barrier for enhanced reliability [2,3]. The completed 1.0µm RDL damascene process is evaluated using a test chip design that includes metrology structures for in-line monitoring and CD-SEM measurements, and comb and serpentine electrical test structures. The electrical results for the damascene process show significant advantages compared to the semi-additive process.

Introduction

Fan-Out wafer level packaging has seen rapid adoption due to its form factor, support for increased interconnect density, and enhanced electrical and thermal package performance. It also provides significant cost advantages compared to interposer and 3D packaging techniques. Redistribution layers (RDL) are used to route high density connections on the chip to lower density connections on the substrate. RDL can also be used to provide interconnection of multiple dies in a package. High density fan-out (HDFO) wafer-level packaging requires multiple layers of RDL to support the necessary routing. Decreasing the metal line critical dimension (CD) to 1.0µm facilitates reducing the number of redistribution levels and decreasing the total packaging cost. However, reducing the RDL pitch requires tightening lithography requirements and enhancing the copper (Cu) electroplating and etching processes. Previous work has shown that the undercut and feature erosion after wet etch of the Cu seed layer presents significant challenges for 1.0 µm RDL structures fabricated using a semi-additive through photoresist electroplating process [1].

A promising technique for fabricating 1.0µm RDL structures is a damascene process which utilizes a photosensitive permanent dielectric material. The standard front end of line (FEOL) damascene approach consists of depositing a dielectric layer, applying photoresist, lithographic patterning, and dry etching to create trenches in the dielectric for Cu electroplating. In order to simplify the damascene process and reduce costs the trenches are created directly in the photosensitive dielectric material which is applied and patterned using standard photoresist processes. After lithography the material is cured by UV exposure followed by a sequence of hard baking steps. A low temperature Ti/Cu seed is deposited followed by a leveling Cu electroplating process. The Cu overburden is removed by Chemical mechanical polish (CMP), and additional CMP is done to remove the top of the dielectric which is rounded by the curing process. All processing is performed on 300mm wafers.

The photosensitive dielectric approach provides advantages for fine patterning. Unlike the semi-additive process in which the Cu seed etch directly affects the Cu line dimensions, the Cu overburden removal for the damascene process does not affect the quality of the embedded Cu lines. Damascene processing will also result in a flat wafer surface. This greatly improves the lithographic performance for subsequent layers because the Depth of Focus (DOF) decreases rapidly for smaller RDL structure sizes. At 1.0µm resolution a typical across wafer DOF is around 3 µm. The Ti seed layer which remains after plating also serves as a Cu diffusion barrier on the sides and bottom for enhanced reliability [2,3].

Lithography Characterization

Lithography is performed on a Veeco-Ultratech AP300E advanced packaging stepper with a Wynne Dyson lens supporting 0.16 to 0.24 variable numerical aperture (NA). [4] This unique design permits the use of broadband illumination from a mercury arc lamp, and the system used in this study has a capability to select different wavelengths: i-line, gh-line or ghi-line. The minimum resolution is 0.8 µm with 0.24 NA. For this study, the exposure is Hg i-line and the NA is adjusted to 0.20 to support a 1.0µm resolution target. The tool is also equipped with a WEE (Wafer Edge Exposure) unit for

exposing the edge of the wafer and a WEP (Wafer Edge Protection) unit for protecting a predefined outer edge of the wafer. The two edge processing techniques are used to precisely remove photoresist on the edge of the wafer where electrical contact is required during electroplating, and to create a protective seal or dam ring to prevent leakage of plating solution during the electroplating step.

For exposure process optimization, a small field test reticle is used to facilitate testing across a range of CDs for line/space and contact patterns. The lines and contacts are arranged to support cross section analysis. Arrangement of patterns in the reticle field is shown in figure 1.

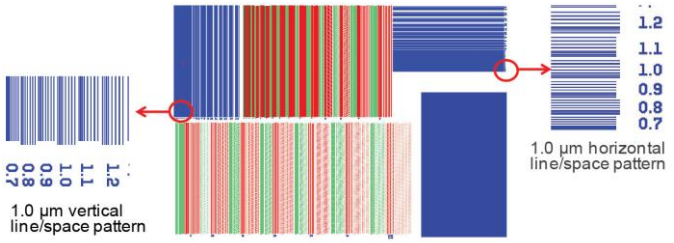

Fig. 1: Reticle UT678B test pattern contains a variety of line/space and square via patterns designed for SEM cross section work.

The photosensitive dielectric material used in this study is manufactured by JSR. The dielectric material has a phenolic resin main polymer and a cross linker to provide chemical resistance for integration processes. It is a chemically amplified negative tone material which requires a post exposure bake (PEB). Development is compatible with 2.38% TMAH developer. After development the material is UV cured followed by a post flood-exposure bake (PFB) performed at a temperature below the glass transition temperature (T_g) which is higher than 200°C. The coefficient of thermal expansion (CTE) of the dielectric material is less than 60ppm. Through the optimization of soft bake, exposure dose, PEB, UV cure, and PFB, smooth sidewalls can be achieved after cure process. The material has a sensitivity to post exposure delay (PED) which affects the pattern profile quality. Longer PED induces poorer profiles, which is due to the deactivation of exposure-generated acids.

The photosensitive dielectric is spin coated to a thickness of 3.0µm on 300 mm Si wafers. The coating is performed using a Suss RC13 manual coater. The lithography process steps are listed in Table 1.

Process Step	Condition
Post Coat Bake	110°C, 120 seconds, contact hotplate
Post Exposure Bake	110°C, 120 seconds, contact hotplate
Develop	90 seconds immersion at room temperature, 2.38% TMAH

Table 1: Photosensitive dielectric process conditions for 3 µm thick JSR photosensitive dielectric material.

A focus/exposure matrix (FEM) is performed to determine the nominal exposure dose and focus using the UT678B reticle and Si wafers. In the FEM wafer layout, the focus offset (µm) is varied along the X-axis while the exposure dose (mJ/cm^2) is varied along the Y-axis as shown in figure 2. This allows a wide range of lithography conditions to be evaluated on a single wafer. The exposure dose and focus offset of the stepper are optimized for 1.0µm line/space using i-line illumination and a lens NA of 0.20. The wafer is cleaved for SEM cross section analysis and a Hitachi S-7840 CD SEM is used to determine the best dose and focus conditions on Si wafer.

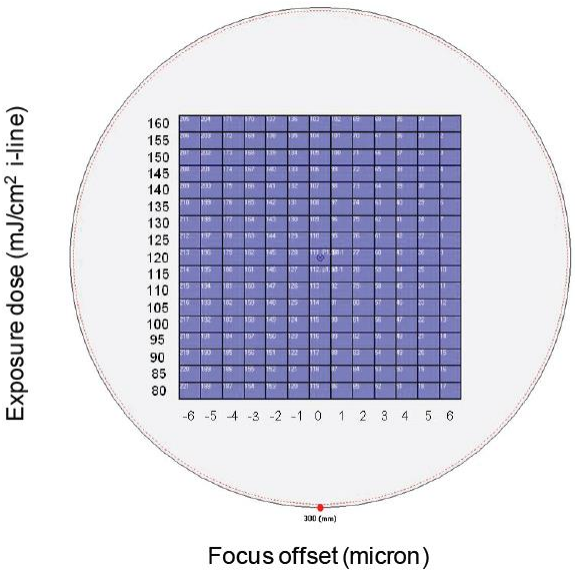

Fig. 2: Wafer layout for the FEM. A thirteen column by seventeen row array of fields was exposed with focus varying in the horizontal axis and exposure varying in the vertical axis.

Top down and cross section SEM images are used to characterize the photosensitive dielectric process and to determine optimum exposure and focus conditions on Si. The SEM data from the FEM wafers on Si is presented in figure 3. Top down SEM images show some residues in the 1.0µm spaces which are acceptable and will be removed in the following descum process.

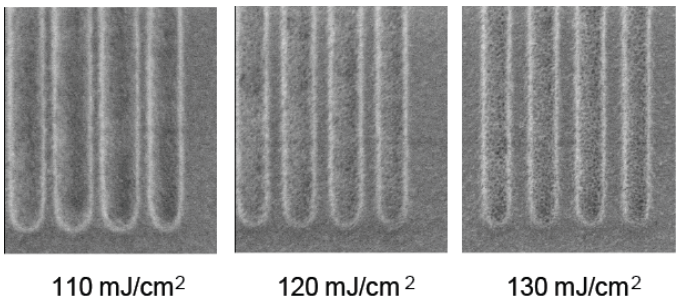

Fig. 3: Top down SEM images of 1µm line/space in 3µm thick JSR photosensitive dielectric on Si through exposure dose, i-line exposure, 0.20 NA.

Top down SEM images of 1.0µm line/space in 3.0µm thick JSR photosensitive dielectric are taken across a range of focus settings at 120 mJ/cm^2 i-line exposure dose as shown in figure 4.

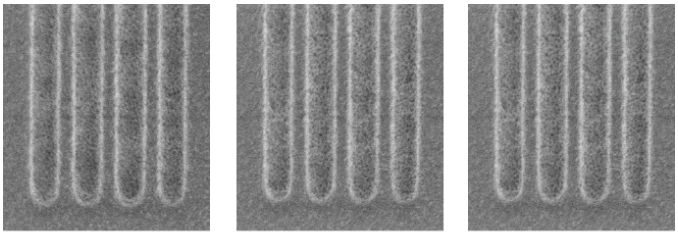

Fig. 4: Top down SEM images of 1.0µm line/space in 3µm thick JSR photosensitive dielectric on Si through focus, i-line exposure, 0.20 NA.

To investigate the damascene process**,** the exposure condition is optimized for SiN deposited on Si substrates to pattern a meandercomb test structure, a long resistor line meandering between fingers. The wafer layout is shown in figure 5. Wafer edge protection (WEP) is used to clear the edge for electrical contact during electroplating.

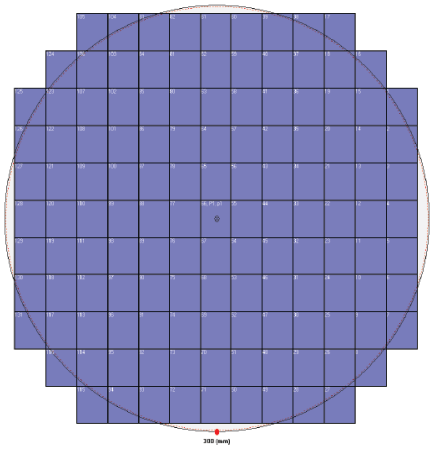

Fig. 5: Layout of 300 mm wafer with wafer edge protection used to clear the edge for electrical contact.

Top down SEM image of a 1.0µm meandercomb structure and SEM cross section of 1.0µm line/space on the SiN on Si substrate after development of the photosensitive dielectric are shown in Figures 6(b) and (a). The 1.0µm space is resolved with some residues which will be removed with descum. The nominal exposure dose with 200nm SiN deposited on Si is 180 mJ/cm^2.

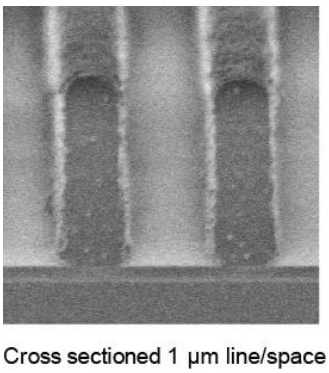

Fig. 6(a): SEM cross sectioned image of 1.0µm line/space in 3µm thick JSR photosensitive dielectric on SiN, i-line exposure, 0.20 NA.

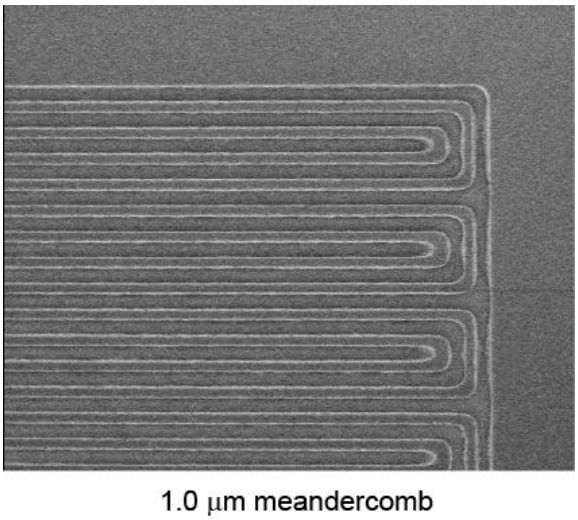

Fig. 6(b): Post development SEM top down view of 1.0µm meandercomb in 3µm thick JSR photosensitive dielectric on SiN, i-line exposure, 0.20 NA.

After development, the photosensitive dielectric is UV cured and baked using the conditions summarized in Table 2. For best pattern profile results there should be no time delay between UV cure and baking.

Process Step	**Condition**
UV Cure	1000 mJ/cm^2 ghi-line, open frame reticle exposure on stepper
Bake	110^{o}C, 900 seconds, contact hotplate
Bake	150^{o}C, 180 seconds, contact hotplate

Table 2: UV cure and bake condition post development. For best pattern profile results there should be no delay between UV exposure and baking.

Test Lot Fabrication

A reticle containing test structures to investigate 1.0µm damascene patterning is used to create electrical test patterns on 300mm wafers. In order to obtain reliable electrical measurements first a silicon nitride passivation layer is deposited on the wafer. The damascene process flow is shown in figure 7.

The photo-sensitive polymer is patterned using the processing conditions described in the previous section. After development the wafers receive a flood UV exposure on the AP300E using a large open field reticle, immediately followed by a Post Flood-exposure Bake (PFB). Exposure, PEB, development, UV-cure and PFB are all executed without delays. At this stage the polymer is semi cured and a final cure to 200°C is performed in a vertical furnace.

For electroplating, a seed layer is deposited at low temperature to avoid wrinkling of the polymer. The polymer is first degassed in-situ at 120°C and a room temperature deposition of 30nm Ti and 150nm Cu seed layer is performed. Subsequently the trenches are filled with electroplated Cu.

The Cu overburden after electroplating is removed using a four step CMP process:

1. Fast bulk Cu removal
2. Slow Cu landing
3. Adhesion/barrier removal
4. Polymer recess

All four process steps utilize dedicated slurries and pads.

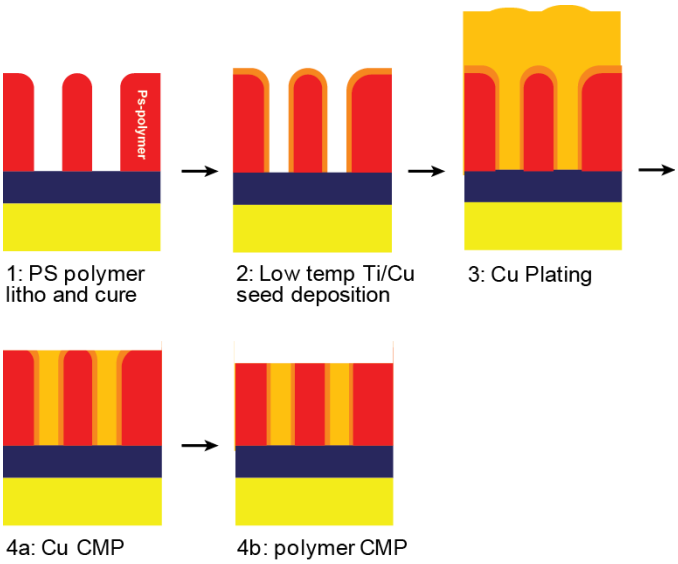

Fig. 7: Fabrication steps for damascene process flow. The resulting meandercomb structures are tested for electrical shorts and resistance.

The performance of the resulting RDL features is evaluated by electrical testing. The primary electrical test structure is a meandercomb, which is a long resistor line meandering between two lines that are not connected to the resistor. In leakage current mode, voltage is applied to one of the resistor line ends while both leakage test fingers are connected to ground, and any leakage between the resistor line and the fingers will result in a measured current. In resistor mode a voltage is applied over the resistor and the resulting current provides an indication of thickness and effective width of the resistor line. Figure 8 depicts the resistor under test in green and the finger structure for leakage current testing in blue.

All resistor structures are designed with a constant length over width (CD) ratio of 2100 to facilitate direct comparison of performance across different structure sizes. The resistor can be represented as 2100 squares with each square having a resistance that depends only on the thickness and specific resistance, regardless of size. Furthermore, we have included multiple instances of these meandercombs with bias of -100nm, 0nm, +100nm and +200nm. The bias refers to the spacewidth in the photosensitive dielectric polymer which becomes the linewidth of the Cu line.

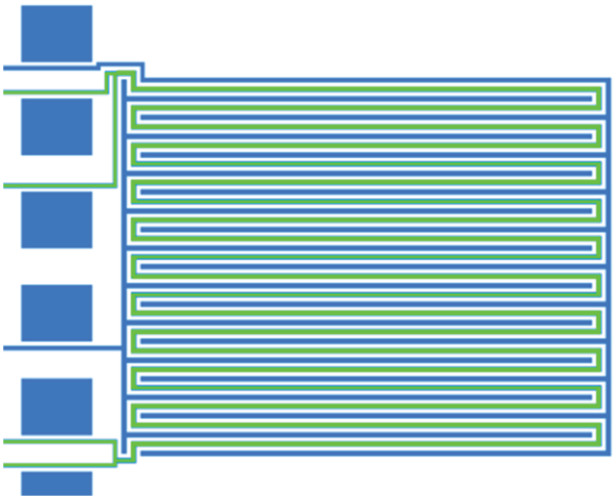

Fig. 8: Meandercomb structure used for electrical testing. The resistor under test is in green and the finger structure for leakage current testing is in blue.

Results and Discussion

After full cure the 1.0µm meandercombs without bias are well defined. The increase in defects for patterns with ±100nm bias indicates that tight CD control is required as can be seen in figure 9. Some top-loss and round-off can be observed for the zero bias case. The -100nm bias case has residues and +100nm bias case exhibits pattern collapse. Since the curing temperature budget is higher than metallization temperature budget the polymer profiles are not affected by the Cu seed deposition and plating.

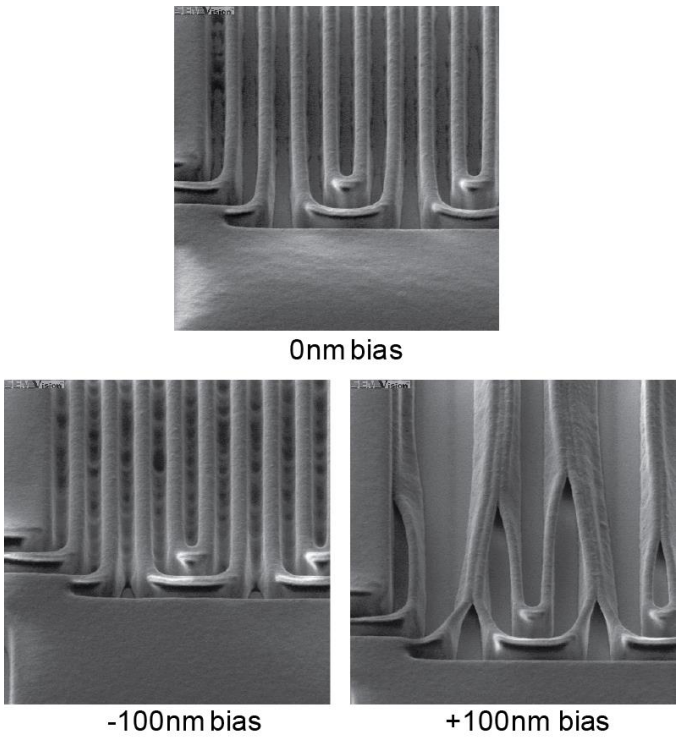

Fig. 9: Pattern fidelity of 1 µm line/space meandercomb in photosensitive dielectric after full cure as a function of bias shows sensitivity to CD change.

Bulk CMP and adhesion layer CMP effectively flatten the surface to provide proper definition for isolated 1.0µm lines. However, spaces for dense lines, and small spaces between much larger features, remain shorted due to polymer top-loss and round-off. Also there appears to be some Cu smearing into the polymer, which can be seen in figure 10. To provide isolation for all features an extra CMP with non-selective slurry is added to remove the round-off and Cu smearing residue.

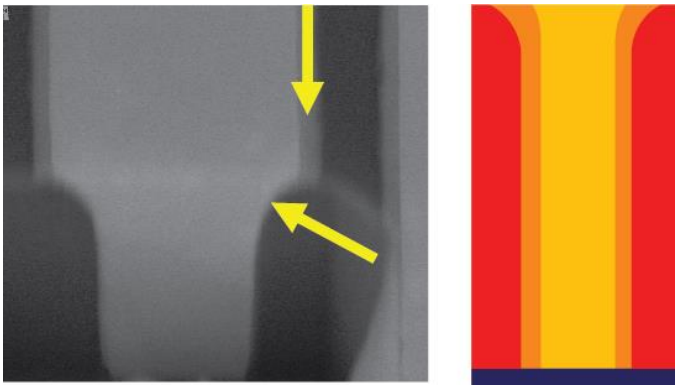

Fig. 10: Dielectric and Cu profile after Cu and barrier CMP. Further recess CMP is required to remove the round-off and Cu smearing. The actual image is compared with the CMP process step 4(a) shown in figure 7.

In the final profile after complete CMP the round-off and Cu smearing has been removed. The full CMP process reduces the polymer and Cu thickness. After full curing the 1.0µm lines are 2.2µm high, and after full CMP the Cu is 1.6µm high as shown in figure 11.

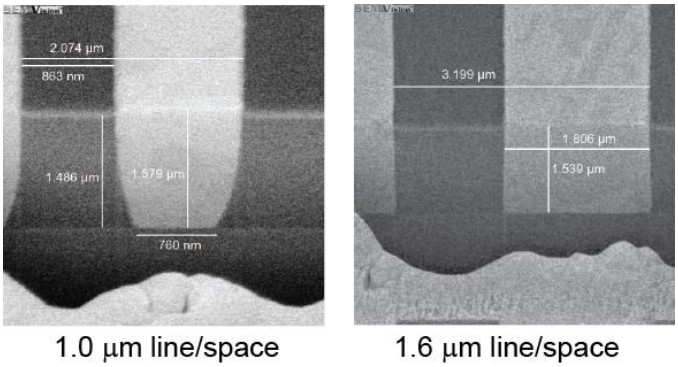

Fig. 11: Focus ion beam cut of 1.0µm and 1.6µm Cu lines after completing the full CMP process.

One observation is that the pattern fidelity of the meandercomb structures is affected by feature size as shown in figure 12. The meandercomb with 1.6µm lines and spaces exhibits some small change in linewidth near bends, line end or T-junctions. However, the meandercomb with 1.0µm lines and spaces has considerably larger pattern deformation. The blue inset indicates the pattern as designed. This indicates that for the combination of photosensitive polymer and stepper we are near the resolution limit; and for improved pattern definition with less deformation OPC may be required.

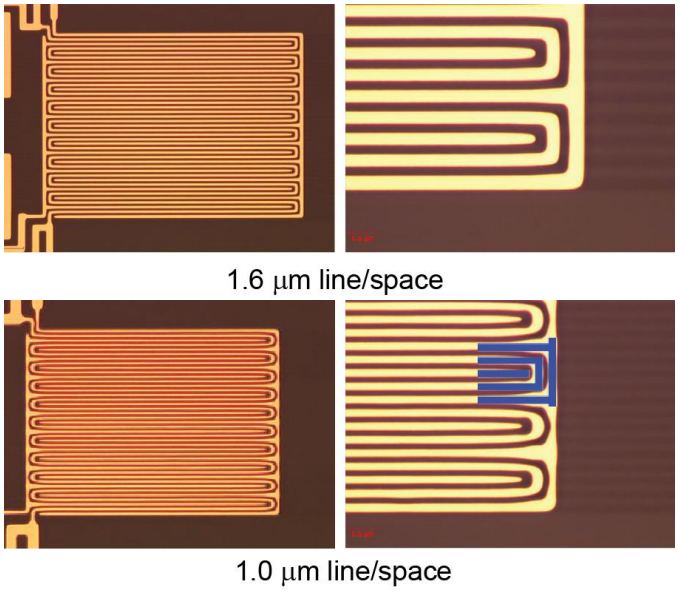

Fig. 12: Top images are of 1.6µm line/space meandercomb, and the bottom images are 1.0µm line/space meandercomb test structure after full CMP process. The blue inset represents design (ideal) pattern.

CD for 1.0µm damascene lines is measured at 41 locations across the wafer and summarized in figure 13. The eight SEM pictures across the wafer show the lines are well defined with no observable edge roughness. The CD averages 1012nm with a 3σ of 105nm. This shows very good CD uniformity across the wafer for the damascene process.

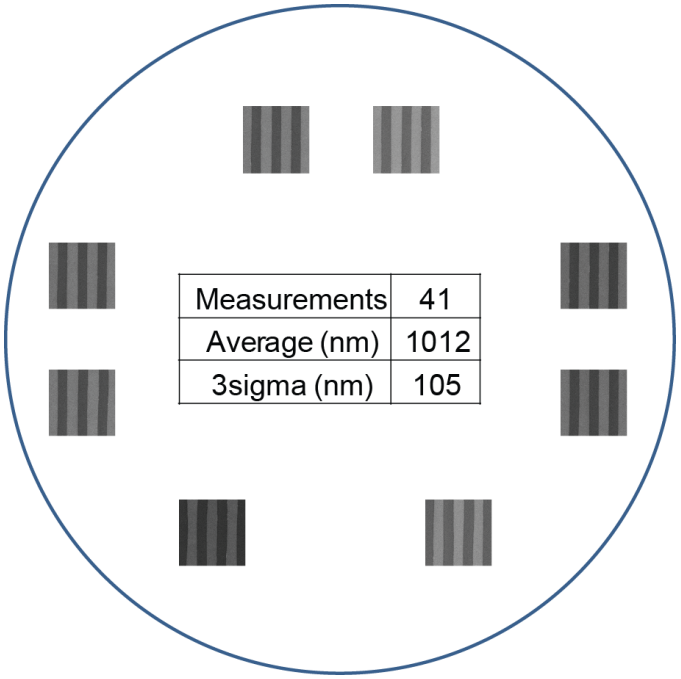

Fig. 13: CD of 1.0µm damascene lines measured at 41 points across wafer averages 1012nm with 3σ of 105nm.

Electrical testing in leakage mode produces high yield of 100% for 1.0µm line/space and 90% for 1.6µm line/space. The lower yield for the larger 1.6µm line/space feature is attributed to accidental FIB cuts prior to electrical testing. For the 1.6µm structures all biases produce good electrical yield, and biasing produces small shifts in average resistance as expected. However, for the 1.0µm structures only the 0nm bias produces proper polymer profiles with 100% yield and a resistance of 22Ω ±3 (3σ). The electrical test data are summarized in figure 14.

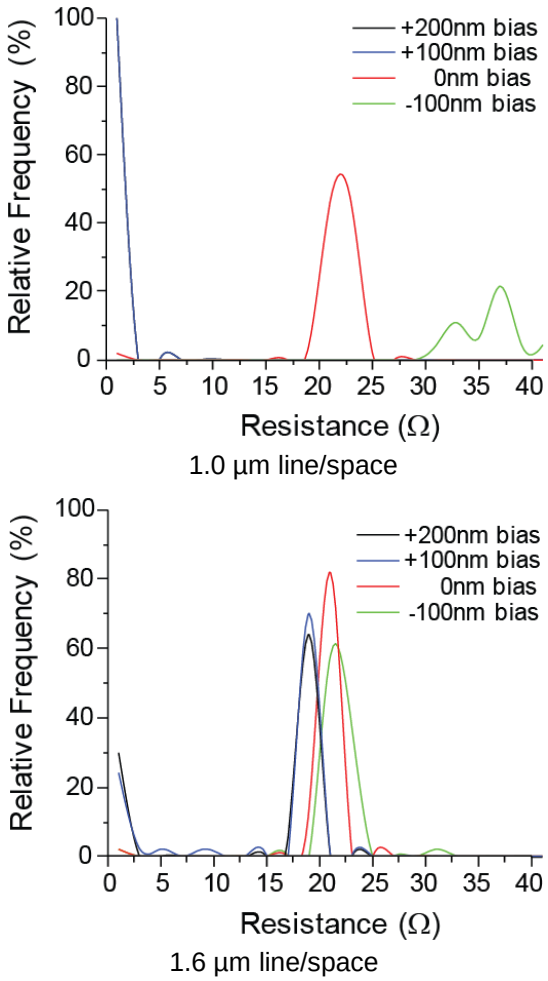

Fig. 14: Electrical testing in leakage mode produces high yield of 100% for 1.0µm line/space and 90% for 1.6µm line/space. The lower yield for the larger 1.6µm structure is attributed to accidental FIB cuts prior to electrical testing.

Conclusions

One micron RDL structures were created using a damascene process which uses a photosensitive permanent dielectric material. This approach avoids the Cu seed etch, used in the traditional semi-additive RDL process, which significantly affects the final Cu line dimensions for smaller feature sizes. The damascene process provides other advantages such as producing a planarized final structure that would improve lithographic performance for subsequent layers, and surrounding the Cu lines with a Ti diffusion barrier to enhance reliability. The damascene process relies primarily on the patterning of the dielectric material to define the final feature size. The CMP process to remove the overburden after Cu plating is also important but does not affect the quality of the Cu lines. SEM images show the patterning of dielectric material and the resulting RDL cross sections after CMP. Good CD uniformity is measured across the wafer. Electrical testing of meandercomb test structures is used to verify performance of one micron RDL structures, and good electrical yield is demonstrated for the optimized 1.0µm process.

Acknowledgments

We would like to thank Nancy Heylen, Lieve Teugels, Bart de Wachter of IMEC for their assistance with the wafer processing and data collection.

References

1. W. Flack et. al., “One Micron Redistribution for Fan-Out Wafer Level Packaging”, *19th Electronics Packaging Technology Conference*, Singapore, 2017.
2. K.W. Paik, “Studies on metal/benzocyclobutene (BCB) interface and adhesion”, *Journal of Adhesion Science and Technology*, Vol. 7, 1993.
3. L. Dumas et. al., “Electromigration and adhesion improvements of Thick Cu/BCB architecture in BiCMOS RF technology”, 2006.
4. Flores, G. et. al, “Lithographic Performance of a New Generation i-line Optical System,” *Optical/Laser Lithography VI Proceedings*, SPIE 1927 (1993).